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EXAMINER

KOBER, RUSSELL MARC

ART UNIT PAPER NUMBER

2829

DATE MAILED: 11/01/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

# Office Action Summary

Application N .

09/844,175

Applicant(s)

FARNWORTH ET AL. *W*

Examiner

Russell M Kobert

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

## Status

- 1) ☒ Responsive to communication(s) filed on 12 August 2002.
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

## Disposition of Claims

- 4) ☒ Claim(s) 31-42 and 54-66 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 31-42 and 54-66 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

## Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on \_\_\_\_\_ is: a) ☐ approved b) ☐ disapproved by the Examiner.  
If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

## Priority under 35 U.S.C. §§ 119 and 120

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  
a) ☐ All b) ☐ Some \* c) ☐ None of:  
1. ☐ Certified copies of the priority documents have been received.  
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.  
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).  
\* See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).  
a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☒ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

## Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892) 4) ☐ Interview Summary (PTO-413) Paper No(s). \_\_\_\_\_
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948) 5) ☐ Notice of Informal Patent Application (PTO-152)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 3-6 & 12. 6) ☐ Other:

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1. Applicant's arguments with respect to claims 31-42 and 54-63 have been considered but are moot in view of the new ground(s) of rejection.

2. Claims 31-42 and 54-63 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

It is not clear to what degree an apex in the form of a knife-edge line is intended to be limited to as mentioned in claims 31, 54 and 66. An apex can be defined in at least two ways as noted in the Collegiate Version of the Meriam-Webster dictionary, Internet address: <http://www.miriamwebster.com/cgi-bin/dictionary>. In one instance an apex is defined as the uppermost point while in another instance an apex is defined as the narrowed or pointed end. Broadly interpreted an apex is understood to be limited to the uppermost point of a structure. Moreover, it is not apparent how sharp the narrowest part of the apex would have to be to form a knife-edge line. Additionally, it is not clear what orientation the knife-edge line resides with respect to the apex. Does the knife-edge line reside in a plane on a rising side of the apex or does the knife-edge line reside in a plane parallel to the base of an apex? Moreover, is a knife-edge line limited to a plane or linear orientation? A knife-edge line can be drawn in a random pattern in three-dimensional space. As a for-instance, a potato chip defines a knife-edge line at its periphery wherein the knife-edge line does not lie in single plane and does not have to be linear. Additionally, it is not clear how narrow an edge of a structure must be to quantify as a knife-edge. Referring once again to the potato chip example, is the edge

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of the potato chip narrow enough to be a knife-edge? For purposes of examination, the examiner has taken the meaning of an apex to be the uppermost portion of an object and an apex having a knife-edge line is understood to be an edge drawn to a line defined by the uppermost portion of an object.

As to claims 62 and 64, it is not clear how the knife-edge line is sized and positioned to extend elevationally above an uppermost surface of the substrate when the uppermost surface of the substrate is located at substrate's uppermost point. In other words, nothing can extend above an uppermost location.

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

(e) the invention was described in-

(1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effect under this subsection of a national application published under section 122(b) only if the international application designating the United States was published under Article 21(2)(a) of such treaty in the English language; or

(2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that a patent shall not be deemed filed in the United States for the purposes of this subsection based on the filing of an international application filed under the treaty defined in section 351(a).

4. Claims 31-37, 39, 54, 55, 57-60, 63, 65 and 66 are rejected under 35 U.S.C. 102(b) as being anticipated by Coberly et al (4116523).

Coberly et al anticipates a removable electrical interconnect apparatus (Figures 1, 4-7 and 8) for removably engaging electrically conductive pads on a semiconductor

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substrate (58; col 3, ln 24-27) having integrated circuitry fabricated therein, the apparatus comprising: a substrate (18, 36); and an engagement probe (circuit contact points 22, 40) projecting from the substrate to engage a single conductive pad on a semiconductor substrate having integrated circuitry formed in the semiconductor substrate, the engagement probe having an outer surface comprising an apex (that portion of probe structures 22 and 40 pointing downward) in the form of at least one knife-edge line (part of blade-like active body member 10; col 2, ln 37-48) configured to removably engage the single conductive pad of the substrate comprising operable integrated circuitry and to removably engage another single conductive pad of another substrate also comprising operable integrated circuitry; as recited in claim 31.

Coberly et al anticipates anticipates a removable engagement probe (Figures 1, 4-7 and 8) having an outer surface comprising an apex (that portion of probe structures 22 and 40 pointing downward) in the form of at least one knife-edge line (part of blade-like active body member 10; col 2, ln 37-48) sized and positioned to engage a single conductive pad; and wherein the knife-edge line projects from a penetration stop plane (see Figures 6 and 7, that portion of 42 adjacent to 40); as recited in claim 54.

As to claims 32 and 55, Coberly et al anticipates the engagement probe is formed on a projection (20, 42) from the substrate (18, 36).

As to claim 33, Coberly et al anticipates the knife-edge line projects from a penetration stop plane (see Figures 6 and 7, that portion of 42 adjacent to 40).

As to claims 34 and 57, Coberly et al anticipates the knife-edge line projects from a penetration stop plane (see Figures 6 and 7, that portion of 42 adjacent to 40), the

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knife-edge line having a tip and having a base at the penetration stop plane, the tip being a distance from the penetration stop plane of about one-half the thickness of the conductive pad which the apparatus is adapted to engage.

As to claims 35 and 58, Coberly et al anticipates the engagement probe is formed on a projection (20, 42) from the substrate (18, 36), the knife-edge line projecting from a penetration stop plane on the projection (see Figures 6 and 7, that portion of 42 adjacent to 40).

As to claims 36 and 59, Coberly et al anticipates the engagement probe is formed on a projection (20, 42) from the substrate (18, 36), the knife-edge line projects from a penetration stop plane on the projection (see Figures 6 and 7, that portion of 42 adjacent to 40), the knife-edge line having a tip and having a base at the penetration stop plane, the tip being a distance from the penetration stop plane of about one-half the thickness of the conductive pad which the apparatus is adapted to engage.

As to claims 37 and 60, Coberly et al anticipates the outermost portions of the electrically conductive apices constitute a first electrically conductive material, wherein the conductive pads for which the apparatus is adapted have outermost portions constituting a second electrically conductive material; the first and second electrically conductive materials being different.

As to claim 39, Coberly et al anticipates the knife-edge line includes an outer conductive layer (col 3, ln 7-10).

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As to claim 63, Coberly et al anticipates the projection having a surface substantially parallel (see bottom portions of 20, 42 and 18, 36) to a surface of the substrate.

As to claim 65, Coberly et al anticipates the projection having a surface substantially parallel (see bottom portions of 20, 42 and 18, 36) to a surface of a substrate which defines the penetration stop plane.

Coberly et al anticipates a removable electrical interconnect apparatus (Figures 1, 4-7 and 8) for removably engaging electrically conductive pads (58; col 3, ln 24-27) on a semiconductor substrate having integrated circuitry fabricated therein, the apparatus comprising:

A substrate (18, 36); and

An engagement probe (circuit contact points 22, 40) projecting from the substrate to engage a single conductive pad on a semiconductor substrate having integrated circuitry formed in the semiconductor substrate, the engagement probe having an outer surface comprising an apex (that portion of probe structures 22 and 40 pointing downward) in the form of at least one knife-edge line (part of blade-like active body member 10; col 2, ln 37-48) sized and positioned to extend elevationally above a surface of the substrate to engage the single conductive pad;

Wherein the engagement probe is formed on a projection (20 and 42) from the substrate, the knife-edge line projects from a penetration stop plane on the projection (see Figures 6 and 7, that portion of 42 adjacent to 40), the knife-edge line having a tip and having a base at the penetration stop plane, the tip being a distance from the

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penetration stop plane of about one-half the thickness of the conductive pad which the apparatus is adapted to engage; as recited in claim 66.

5. Claims 31, 39 and 40 are rejected under 35 U.S.C. 102(b) as being anticipated by Stowers (4417206).

Stowers anticipates a removable electrical interconnect apparatus (Figure 1) for removably engaging electrically conductive pads on a semiconductor substrate having integrated circuitry fabricated therein, the apparatus comprising:

a substrate (10); and an engagement probe (that portion of structure 10 protruding toward point 21) projecting from the substrate to engage a single conductive pad on a semiconductor substrate having integrated circuitry formed in the semiconductor substrate, the engagement probe having an outer surface comprising an apex (22 and/or 22a) in the form of at least one knife-edge line (edge formed at top of apexes 22 and 22a) configured to removably engage the single conductive pad of the substrate comprising operable integrated circuitry and to removably engage another single conductive pad of another substrate also comprising operable integrated circuitry; as recited in claim 31.

As to claim 39, Stowers anticipates the knife-edge line includes an outer conductive layer.

As to claim 40, Stowers anticipates the outer surface includes plural knife-edge lines (edges formed at top of apexes 22 and 22a) configured to engage the single conductive pad.



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6. Claims 31-42, 54-61, 63 and 65-66 are rejected under 35 U.S.C. 102(e) as being anticipated by Leedy (5323035).

Leedy anticipates a removable electrical interconnect apparatus (Figures 1b and 2 using the insertion structure of Figure 9) for removably engaging electrically conductive pads (30) on a semiconductor substrate (the IC portion shown under pad 30) having integrated circuitry fabricated therein, the apparatus comprising: a substrate (40); and an engagement probe (that portion of structure 10 below 14) projecting from the substrate to engage a single conductive pad (30) on a semiconductor substrate (IC; col 2, ln 40-42) having integrated circuitry (IC = Integrated Circuit) formed in the semiconductor substrate, the engagement probe having an outer surface comprising an apex (that portion of insertion structure pointing downward) in the form of at least one knife-edge line (136) configured to removably engage the single conductive pad of the substrate comprising operable integrated circuitry and to removably engage another single conductive pad of another substrate also comprising operable integrated circuitry (col 1, ln 25-31); as recited in claim 31.

Leedy anticipates a removable engagement probe (Figures 1b and 2 using the insertion structure of Figure 9) having an outer surface comprising an apex (that portion of insertion structure pointing downward) in the form of at least one knife-edge line (136) sized and positioned to engage a single conductive pad (30); and wherein the knife-edge line projects from a penetration stop plane (that portion of 134

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between knife-edge line portions 136 and/or that portion of 20 horizontal and parallel to 14); as recited in claim 54.

As to claims 32 and 55, Leedy anticipates the engagement probe is formed on a projection (14) from the substrate (40).

As to claim 33, Leedy anticipates the knife-edge line projects from a penetration stop plane (that portion of 134 between knife-edge line portions 136 and/or that portion of 20 horizontal and parallel to 14).

As to claims 34 and 57, Leedy anticipates the knife-edge line projects from a penetration stop plane (that portion of 134 between knife-edge line portions 136 and/or that portion of 20 horizontal and parallel to 14), the knife-edge line having a tip and having a base at the penetration stop plane, the tip being a distance from the penetration stop plane of about one-half the thickness of the conductive pad which the apparatus is adapted to engage (col 3, ln 10-17).

As to claims 35 and 58, Leedy anticipates the engagement probe is formed on a projection (14) from the substrate (40), the knife-edge line projecting from a penetration stop plane on the projection (that portion of 134 between knife-edge line portions 136 and/or that portion of 20 horizontal and parallel to 14).

As to claims 36 and 59, Leedy anticipates the engagement probe is formed on a projection (14) from the substrate (40), the knife-edge line projects from a penetration stop plane on the projection (that portion of 134 between knife-edge line portions 136 and/or that portion of 20 horizontal and parallel to 14), the knife-edge line having a tip and having a base at the penetration stop plane, the tip being a distance from the

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penetration stop plane of about one-half the thickness of the conductive pad which the apparatus is adapted to engage (col 3, ln 10-17).

As to claims 37 and 60, Leedy anticipates the outermost portions of the electrically conductive apexes constitute a first electrically conductive material, wherein the conductive pads for which the apparatus is adapted have outermost portions constituting a second electrically conductive material; the first and second electrically conductive materials being different (col 2, ln 66 – col3, ln 2, 40-46).

As to claims 38 and 61, Leedy anticipates the engagement probe is formed from a semiconductor substrate (col 3, ln 49 - col 5, ln 31).

As to claim 39, Leedy anticipates the knife-edge line includes an outer conductive layer (20).

As to claim 40, Leedy anticipates the outer surface includes plural knife-edge lines (col 5, ln 38-40) configured to engage the single conductive pad.

As to claim 41, Leedy anticipates the engagement probe is formed from a semiconductor substrate (col 3, ln 49 - col 5, ln 31) and the outer surface includes plural knife-edge lines (col 5, ln 38-40) configured to engage the single conductive pad.

As to claim 42, Leedy anticipates the engagement probe is formed from a semiconductor substrate (col 3, ln 49 - col 5, ln 31) and the outer surface includes plural knife-edge lines (col 5, ln 38-40) configured to engage the single conductive pad and the knife-edge lines include outer conductive layers (20, 21).

As to claim 56, Leedy anticipates the outer surface comprises a plurality of apexes having respective tips and bases, and the penetration stop plane is intermediate

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the bases and substantially parallel to a surface of a substrate (that portion of 134 between knife-edge line portions 136 and/or that portion of 20 horizontal and parallel to 14 between the apexes shown in Figure 2).

As to claim 63, Leedy anticipates the projection having a surface substantially parallel (that portion of 134 between knife-edge line portions 136 and/or that portion of 20 horizontal and parallel to 14 between the apexes shown in Figure 2) to a surface of the substrate.

As to claim 65, Leedy anticipates the projection having a surface substantially parallel (that portion of 134 between knife-edge line portions 136 and/or that portion of 20 horizontal and parallel to 14 between the apexes shown in Figure 2) to a surface of a substrate which defines the penetration stop plane.

Leedy anticipates a removable electrical interconnect apparatus (Figures 1b and 2 using the insertion structure of Figure 9) for removably engaging electrically conductive pads (30) on a semiconductor substrate (the IC portion shown under pad 30) having integrated circuitry fabricated therein, the apparatus comprising:

A substrate (40); and

An engagement probe (that portion of structure 10 below 14) projecting from the substrate to engage a single conductive pad (30) on a semiconductor substrate (IC; col 2, ln 40-42) having integrated circuitry (IC = Integrated Circuit) formed in the semiconductor substrate, the engagement probe having an outer surface comprising an apex (that portion of insertion structure pointing downward) in the form of at least one

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knife-edge line (136) sized and positioned to extend elevationally above a surface (border between 40 and 14) of the substrate to engage the single conductive pad;

Wherein the engagement probe is formed on a projection (14) from the substrate, the knife-edge line projects from a penetration stop plane on the projection, the knife-edge line having a tip and having a base at the penetration stop plane (that portion of 134 between knife-edge line portions 136 and/or that portion of 20 horizontal and parallel to 14 between the apexes shown in Figure 2), the tip being a distance from the penetration stop plane of about one-half the thickness of the conductive pad which the apparatus is adapted to engage (col 3, ln 10-17); as recited in claim 66.

7. A shortened statutory period for response to this action is set to expire three month(s) from the date of this letter. Failure to respond within the period for response will cause the application to become abandoned. 35 U.S.C. 133

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Russell Kobert whose telephone number is (703) 308-5222.

Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist whose telephone number is (703) 308-0956.



Russell M. Kobert  
Patent Examiner  
Group Art Unit 2829  
October 24, 2002



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